Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2025

Fifth Semester

Electronics and Communication Engineering

EC3552 - VLSI and Chip Design

Regulations - 2021

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Define body bias effect. How does it influence the threshold voltage of a MOS transistor?	L2	1	2
2.	What is latch up? How to prevent latch up?	L2	1	2
3.	Define Elmore's constant.	L1	2	2
4.	Construct a 2 input XOR using nMOS pass transistor logic.	L2	2	2
5.	Define clock jitter.	L1	3	2
6.	Compare and contrast synchronous design and asynchronous design.	L2	3	2
7.	Mention the need of sense amplifier in memory cell.	L1	4	2
8.	Identify why barrel shifter is very useful in designing of arithmetic circuits?	L2	4	2
9.	List the common techniques involved in adhoc testing.	L1	5	2
10.	What is BIST?	L2	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Explain DC transfer characteristics of CMOS inverter with necessary conditions for different regions of operations.	L3	1	16
			Or			
	b	i	Illustrate the principle of constant field scaling and lateral scaling and also write its effect on device characteristics.	L3	1	8
		ii	Elaborate the C-V characteristics of MOS transistor.	L3	1	8
12.	a	i	Explain the basic principle of transmission gate in CMOS design.	L3	2	8
		ii	Write Short notes on low power design principles.	L2	2	8
			Or			

	b		Explain the layout design rules and draw layout diagram for four input NAND gate.	L3	2	16
13.	a	i	Discuss in detail about the C^2MOS (Clocked CMOS) register.	L3	3	8
		ii	Elaborate in detail about the synchronous design.	L3	3	8
			Or			
	b		Discuss in detail about various pipelining approaches to optimize sequential circuit.	L3	3	16
14.	a		Draw the structure of ripple carry adder and explain its operation. Mention how the ripple carry adder is overcome by carry look ahead adder.	L3	4	16
			Or			
	b	i	Describe the hardware architecture of a 4 bit unsigned array multiplier.	L3	4	8
		ii	Elaborate in detail the design of a 4 bit barrel shifter.	L3	4	8
15.	a	i	Discuss in detail about fault model in testing.	L3	5	8
		ii	Explain about semi custom ASIC with its types.	L3	5	8
			Or			
	b		Explain about design for testability and scan design approaches.	L3	5	16